Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A semiconductor device comprising:

an oxide high-dielectric-constant or ferroelectric film;

a lower capacitor electrode provided under said film; and

an upper capacitor electrode provided on said film and being subjected to a hydrogen atmosphere during manufacturing,

wherein said upper capacitor electrode consists essentially of a metal element in pure metal form selected from a group consisting of palladium, ruthenium, iridium, and nickel, and an additional impurity element having an action of suppressing the catalytic activity of said metal element, wherein said additional element exists as a component of a compound of said pure metal covering a polycrystalline grain surface of said pure metal.

2. (Original) A semiconductor device according to claim 1, wherein said impurity element is any one of lead, sulfur, selenium, tellurium, silicon, phosphorus, arsenic, boron, bismuth, and barium.

3. (Currently Amended) A semiconductor device according to claim 1, wherein the concentration of said impurity element in said upper capacitor electrode is 10 atom% or less.

4. (Withdrawn) A semiconductor device according to claim 1, wherein said lower electrode consists essentially of a metal element in pure metal form selected from a group consisting of palladium, ruthenium, iridium, and nickel.

5. (Currently Amended) A semiconductor device comprising:

an oxide high-dielectric-constant or ferroelectric film;

a lower capacitor electrode provided under said film; and

an upper capacitor electrode provided on said film and being subjected to a hydrogen atmosphere during manufacturing,

wherein said upper capacitor electrode consists essentially of platinum, and an additional element which suppresses the catalytic activity of the platinum and which comprises any one of sulfur, selenium, tellurium, silicon, phosphorus, arsenic, boron and bismuth, wherein said additional element exists as a component of a compound of said platinum covering a polycrystalline grain surface of said platinum.

6. (Currently Amended) A semiconductor device comprising:

a capacitor structure having a lower electrode, an oxide high-dielectric-constant or ferroelectric thin film and ~~a metal~~ an upper metal electrode,

wherein surfaces of ~~polycrystal~~ polycrystalline grains of ~~the~~ metal mainly

contained in said upper metal electrode of said capacitor, formed after formation of said oxide high-dielectric-constant or ferroelectric thin film, are covered with a compound of said metal and another element ~~having~~, wherein said compound of said metal and said another element has an effect of suppressing the catalytic activity of said metal.

7. (Currently Amended) A semiconductor device according to claim 6, wherein said ~~electrode~~ metal of the upper electrode is platinum, and said compound is any one of Pt_3Pb, PtS, Pt_5Se_4, PtTe, Pt_3Si, P_2Pt_5, $PtAs_2$, BPt_3, BiPt, $BaPt_5$, and Pt_3Pb.

8. (Original) A semiconductor device according to claim 6, wherein said high-dielectric-constant or ferroelectric thin film is made from an oxide mainly containing an element selected from a group consisting of barium, lead, strontium, and bismuth.

9. (Currently Amended) A semiconductor memory including a memory cell comprising a MISFET, having a pair of semiconductor regions and a gate electrode, and a capacitor formed on a principal plane of a semiconductor substrate, said capacitor comprising:

a lower electrode electrically connected to one of said semiconductor regions of said MISFET;

an oxide high-dielectric-constant or ferroelectric film ~~form~~ formed on the surface of said lower electrode;

an upper electrode formed on the surface of said oxide high-dielectric-constant or ferroelectric film, said upper electrode mainly containing a metal element selected from a group consisting of palladium, ruthenium, iridium, and nickel and additionally containing an impurity element having an action of suppressing the ~~catalyst~~ catalytic activity occurred on the surface of said oxide high-dielectric-constant or ferroelectric film, wherein said additional element exists as a component of a compound of said metal covering a polycrystalline grain surface of said metal;

an insulating film formed in such a manner as to cover said upper electrode; and

a refractory metal layer connected to said upper electrode via an opening formed in said insulating film.

10. (Original) A semiconductor memory according to claim 9, wherein said impurity element is any one of lead, sulfur, selenium, tellurium, silicon, phosphorus, arsenic, boron, bismuth, and barium.

11. (Original) A semiconductor memory according to claim 9, wherein said lower electrode is a storage electrode, and said upper electrode is a plate electrode.

12. (Original) A semiconductor memory according to claim 9, wherein the concentration of said impurity element in said upper electrode is in a range of 10 atom% or less.

13. (Currently Amended) A semiconductor memory according to claim 9, wherein said impurity element is not added to said lower electrode.

14. (Original) A semiconductor memory according to claim 9, wherein said refractory metal is tungsten.

15. (Currently Amended) A semiconductor memory including a memory cell comprising a MISFET having a pair of semiconductor regions and a gate electrode, and a capacitor formed on a principal plane of a semiconductor substrate, said capacitor comprising:

a lower electrode electrically connected to one of said semiconductor regions of said MISFET;

an oxide high-dielectric-constant or ferroelectric film formed on the surface of said lower electrode;

an upper electrode mainly containing platinum, and additionally containing an element which suppresses the catalytic activity of said upper electrode and comprises any one of impurity of sulfur, selenium, tellurium, silicon, phosphorous, arsenic, boron and bismuth, wherein the additional element exists as a component of a compound of said platinum covering a polycrystalline grain surface of said platinum;

an insulating film formed in such a manner as to cover said upper electrode; and

a refractory metal layer connected to said upper electrode via an opening formed in said insulating film.

16. (Original) A semiconductor memory according to claim 15, wherein said lower electrode is a storage electrode, and said upper electrode is a plate electrode.

17. (Original) A semiconductor memory according to claim 15, wherein the concentration of said impurity element in said upper electrode is in a range of 10 atom% or less.

18. (Currently Amended) A semiconductor memory according to ~~claim 15 or 16, wherein~~ claim 15, wherein said impurity element is not added to said lower electrode.

19. (Currently Amended) A semiconductor memory according to ~~claim 15 or 16, wherein~~ claim 15, wherein said refractory metal is tungsten.

20. (Original) A semiconductor memory according to claim 16, wherein the concentration of said impurity element in said upper electrode is in a range of 10 atom% or less.

21. (Original) A semiconductor memory according to claim 20, wherein said impurity element is not added to said lower electrode.

22. (Original) A semiconductor memory according to claim 20, wherein said refractory metal is tungsten.